D/A Converters

Nyquist-Rate D/A Converts

- Four main types
  - Decoder-based
  - Binary-weighted
  - Thermometer-code
  - Hybrid

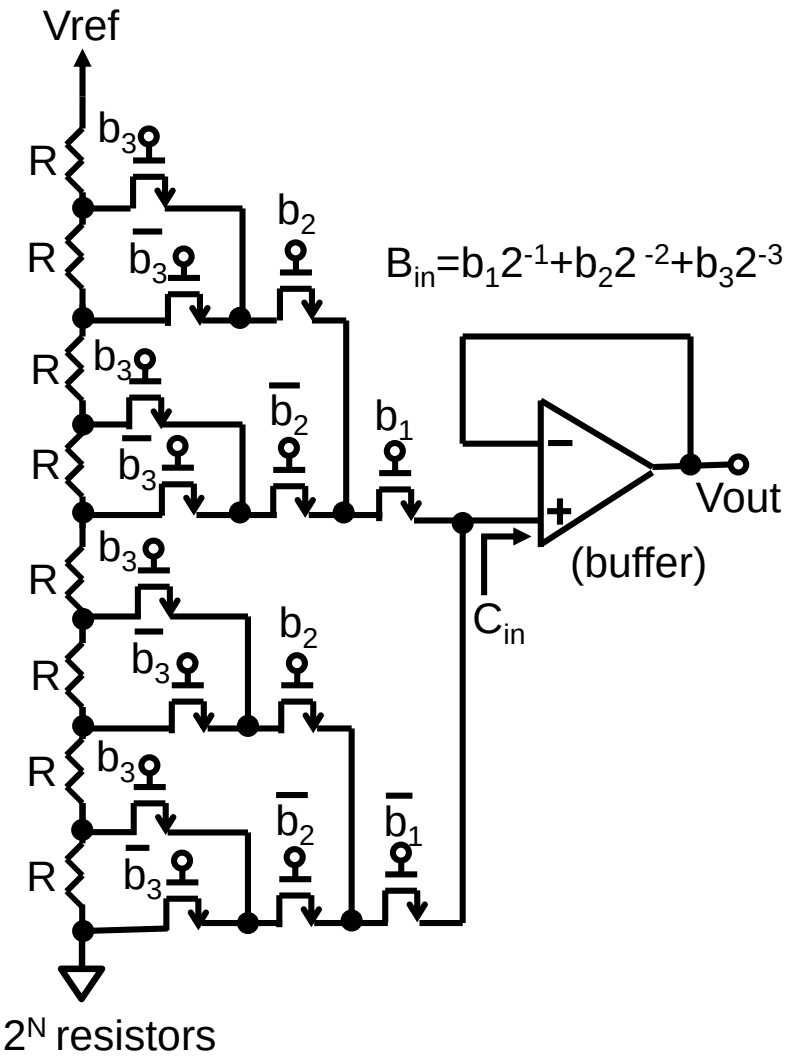
Decoder-Based DAC

- Most straight forward approach
  - Create 2^N reference signals and pass the appropriate signal to the output

- Three main types
  - Resistor string
  - Folded resistor-string
  - Multiple resistor-string

Resistor-String DAC

- Example 1: a 3-bit DAC with transmission-gate, tree-like decoder
  - Transmission gates might be used rather than n-channel switches
    - Extra drain and source capacitance (to GND) is offset by the reduced switch resistance
    - Larger layout
    - Can operate closer to positive supply voltage
  - Only n-channel switches are used
    - About the same speed as the transmission gate implementation
    - Compact layout (no contacts are required in the tree)



Resistor-String DAC (Cont.)

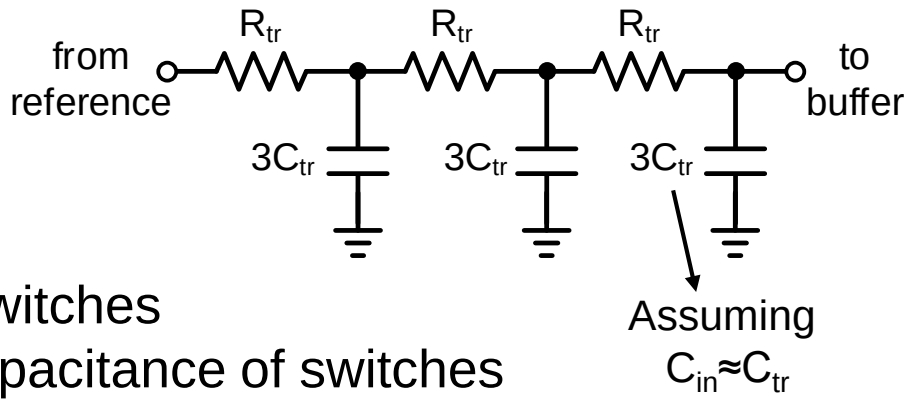
- Monotonicity is guaranteed (if the buffer's offset does not depend on its input voltage)
- The accuracy of this DAC depends on the type of resistor used. Polysilicon (20-30 Ω/square) have up to 10-bit of matching accuracy.
- Speed:

  Can be estimated using open-circuit time-constant approach (refer to microelectronics textbook by Sedra and Smith V.7 p.733, Ch.9)

Time constant

$$\approx 3R_{tr}C_{tr}+2\times 3R_{tr}C_{tr}+\ldots+N\times 3R_{tr}C_{tr}$$

$$=\frac{N(N+1)}{2}\times 3\,R_{tr}C_{tr}$$



where R_{tr} is on resistance of switches

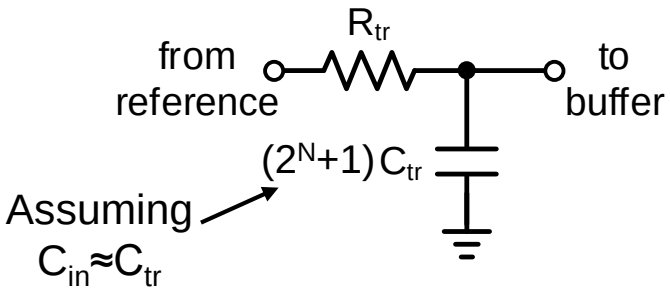
C_{tr} is drain or source capacitance of switches

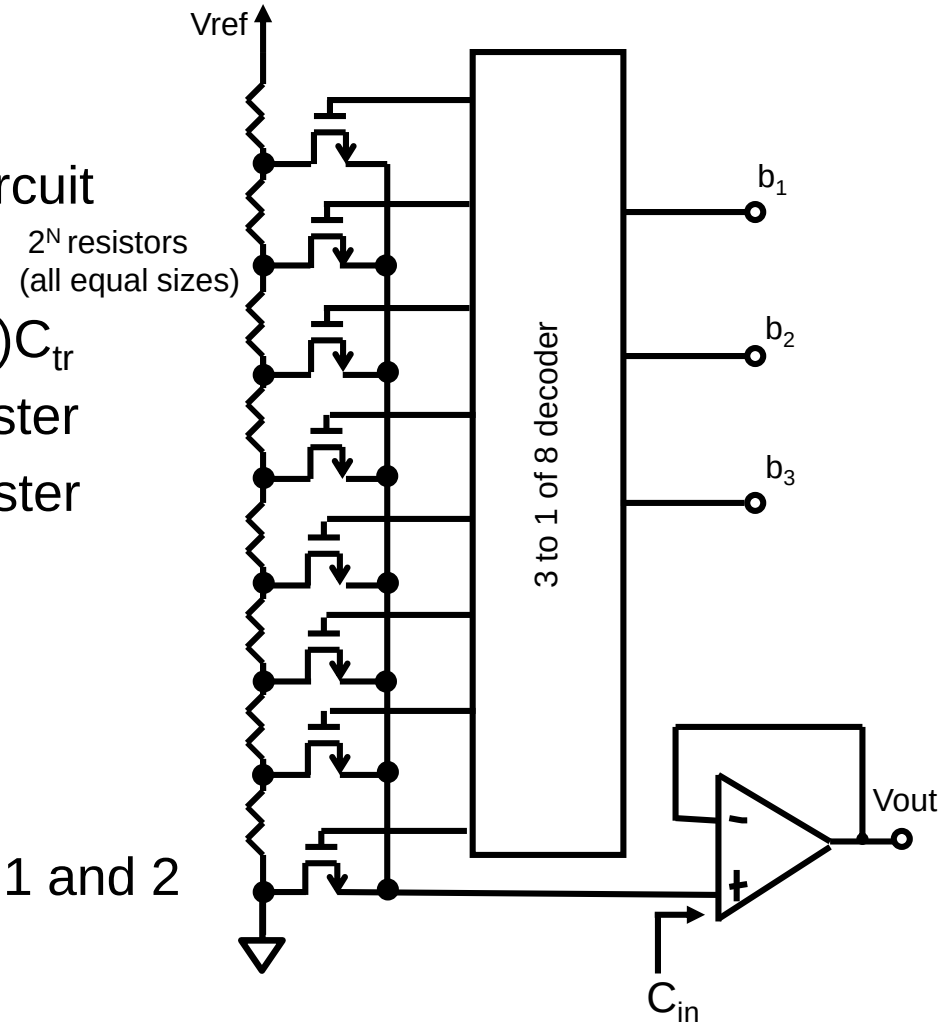
N is bit number

e.g. N=6 → $63R_{tr}C_{tr}$, N=7 → $84R_{tr}C_{tr}$

Resistor-String DAC (cont.)

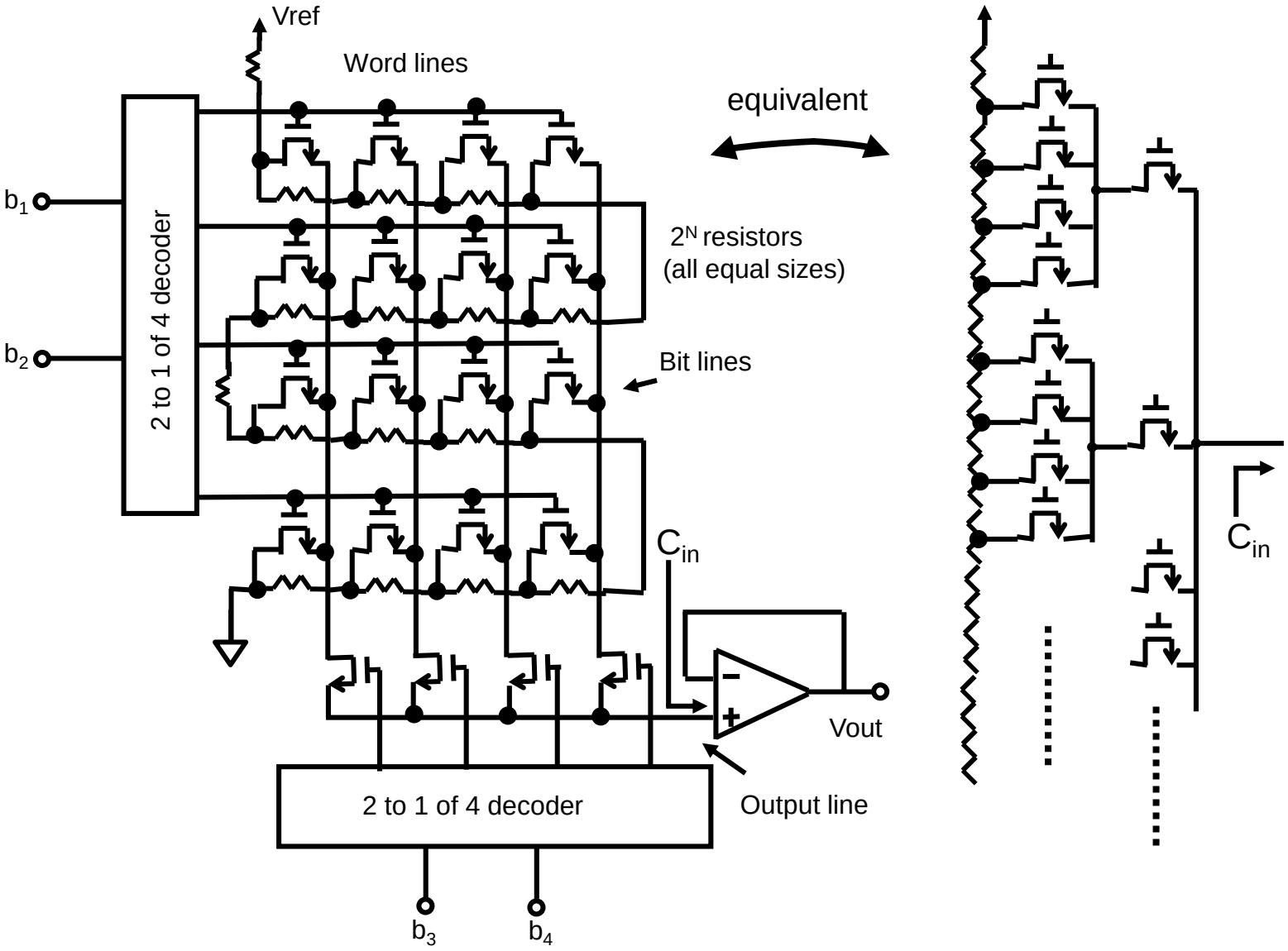
- Example 2: a 3-bit DAC with digital decoding
  - Compared to Example1
    - Higher speed
    - More area for decoding circuit
  - Speed:
    - Time constant $\approx R_{tr} \bullet (2^N+1)C_{tr}$
    - For $N \leq 6$ Example 2 is faster
    - For $N > 7$ Example 1 is faster





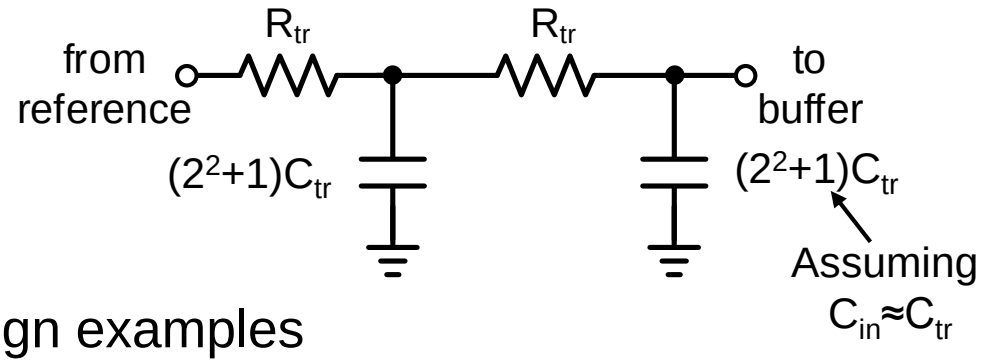
- Compromise between Examples 1 and 2
  - Folded resistor-string DAC

Folded Resistor-String DAC



Folded Resistor-String DAC (Cont.)

- Reduce the amount of digital decoding
- Reduce large capacitive loading
- Decoding is very similar to that for a digital memory
- Example:
  - 4 bits (=2 bits+2 bits) DAC
  - Time constant ≈ R_{tr} $(2^2+1)C_{tr}$+2 R_{tr} $(2^2+1)C_{tr}$

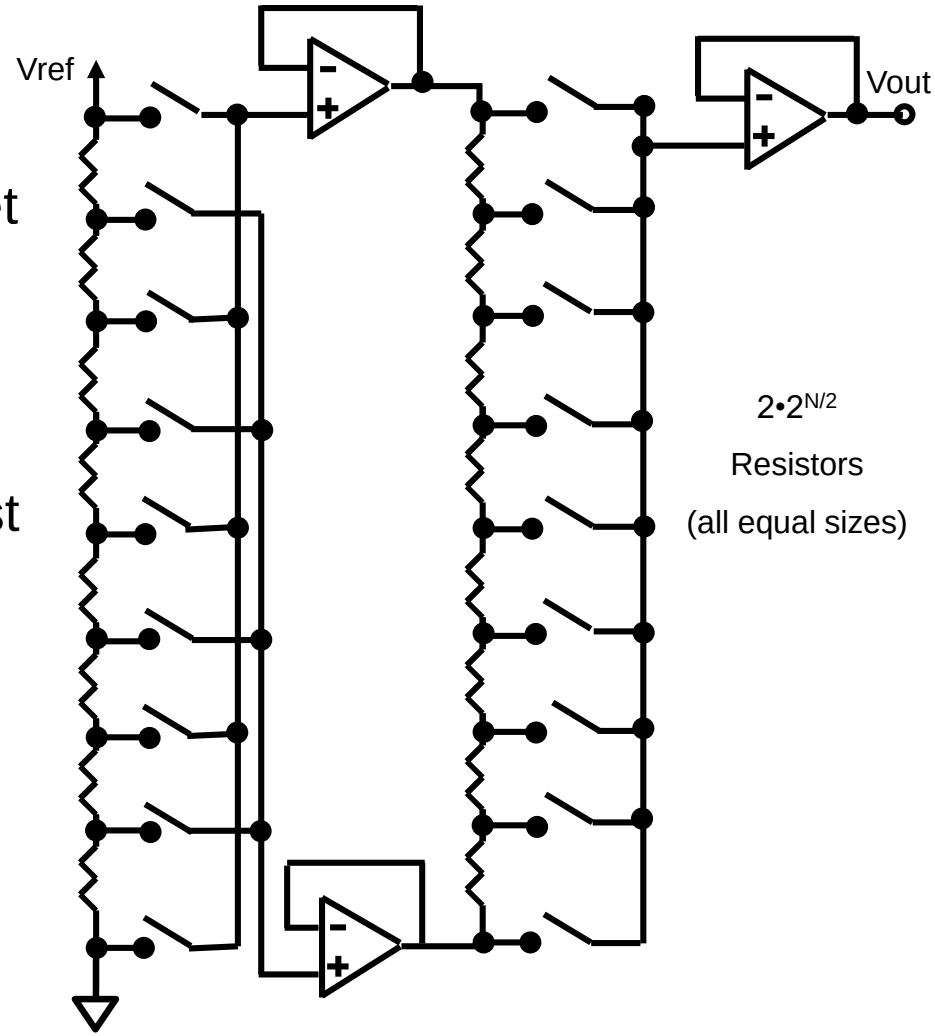


- Other design examples
  - 12 bits=6 bits+6 bits, or 4 bits+4 bits+4 bits, or…..
  - 10 bits=5 bits+5 bits, or 3 bits+3 bits+4 bits, or…...

  ⋮ etc.

Multiple Resistor-string DAC

- 6-bit example
- Requires only $2 \cdot 2^{N/2}$ resistors
- Monotonic if OPAMPs have matched, voltage-insensitive offset voltages.
- For high speed, OPAMPs must be fast.
- For high resolution, OPAMPs must be low noise.
- The matching requirements of the second resistor string are not nearly as severe as those for the first string.



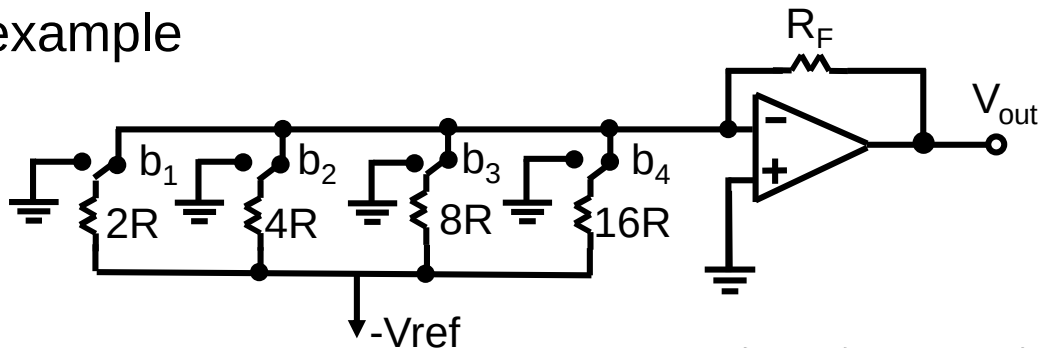
Binary-Weighted (or Binary-Scaled) Converters

- An appropriate set of signals that are all related in a binary fashion
  The binary array of signals might be voltages, charges, or currents

- Binary-weighted resistor DAC
  Reduced-resistance-ratio ladders
  R-2R-based DAC
  Charge-redistribution switched-capacitor DAC
  Current-mode DAC

Binary-Weighted Resistor DAC

- 4-bit example



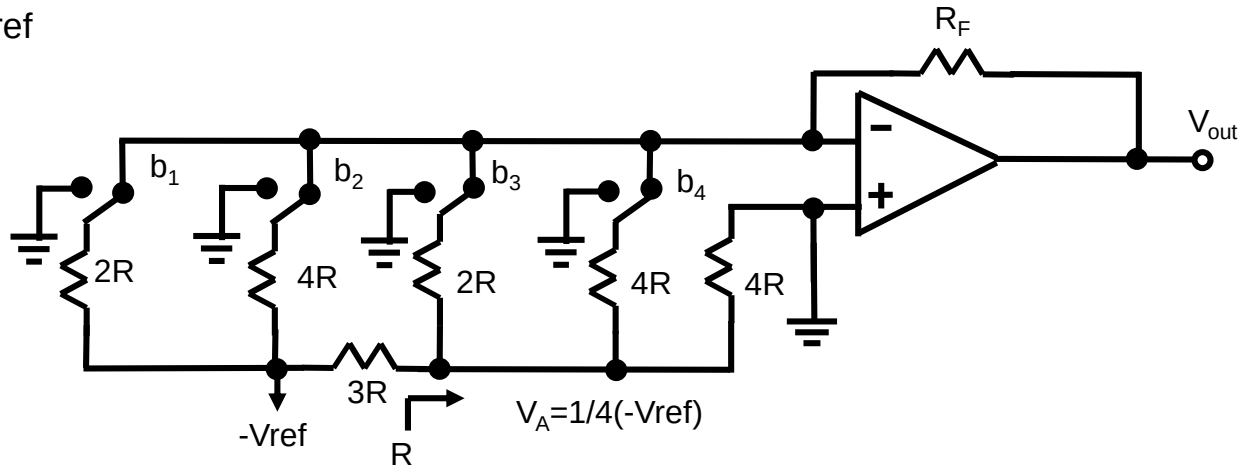
$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} + \cdots\right) = \left(\frac{R_F}{R} V_{ref}\right) B_{in}$$

$$\text{where} \quad B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

- If it does not be integrated in an IC, it would not require many resistors or switches.
- Disadvantages
  - Resistor ratio and current ratio are on the order of 2^N. If N is large, this large current ratio requires that the switches also be scaled so that equal voltage drops appear across them.
  - Monotonicity is not guaranteed
  - Prone to glitches

Reduced-Resistance-Ratio Ladders

- Reduce the large resistor ratios in a binary-weighted array
- Introduce a series resistor to scale signals in portions of the array V_A=-1/4 V_{ref}



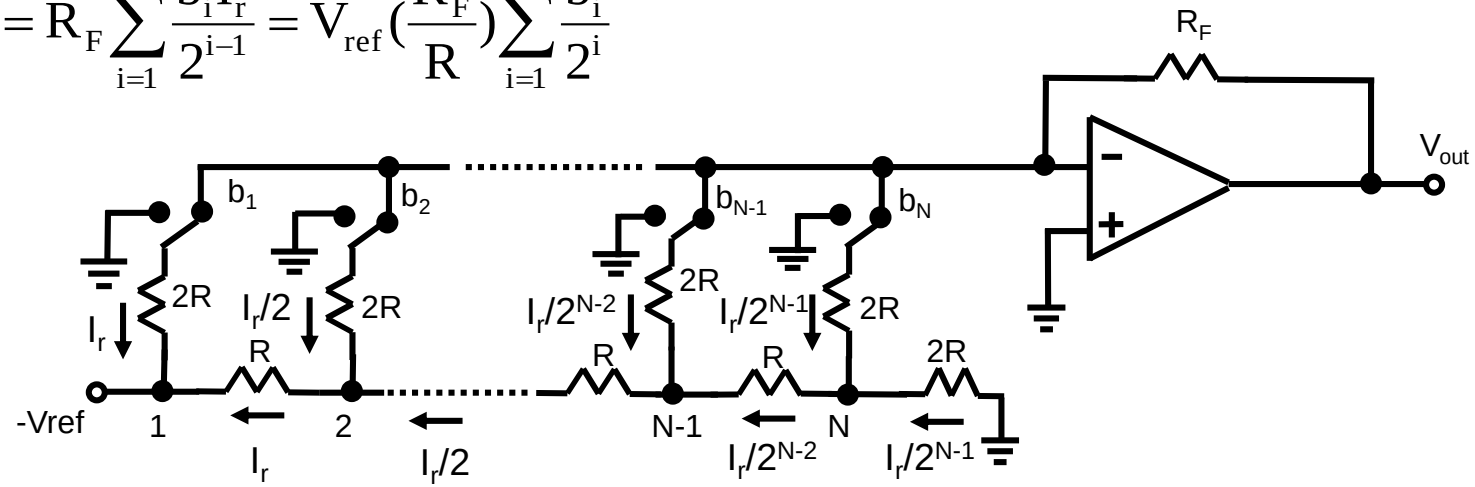
- An additional 4R was added such that resistance seen to the right of the 3R equals R.
- One-fourth the resistance ratio compared to the binary-weighted case
- Current ratio has remained unchanged
  - Switches must be scaled in size
- Repeating this procedure recursively, one can obtain an R-2R ladder

R-2R-Based DAC

- Smaller size and better accuracy than a binary-sized approach
  - Small number of components
  - Resistance ratio of only 2
- 4-bit example

$$I_r = \frac{V_{ref}}{2R}$$

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right)\sum_{i=1}^{N} \frac{b_i}{2^i}$$



- Current ratio is still large
  - Large ratio of switch sizes

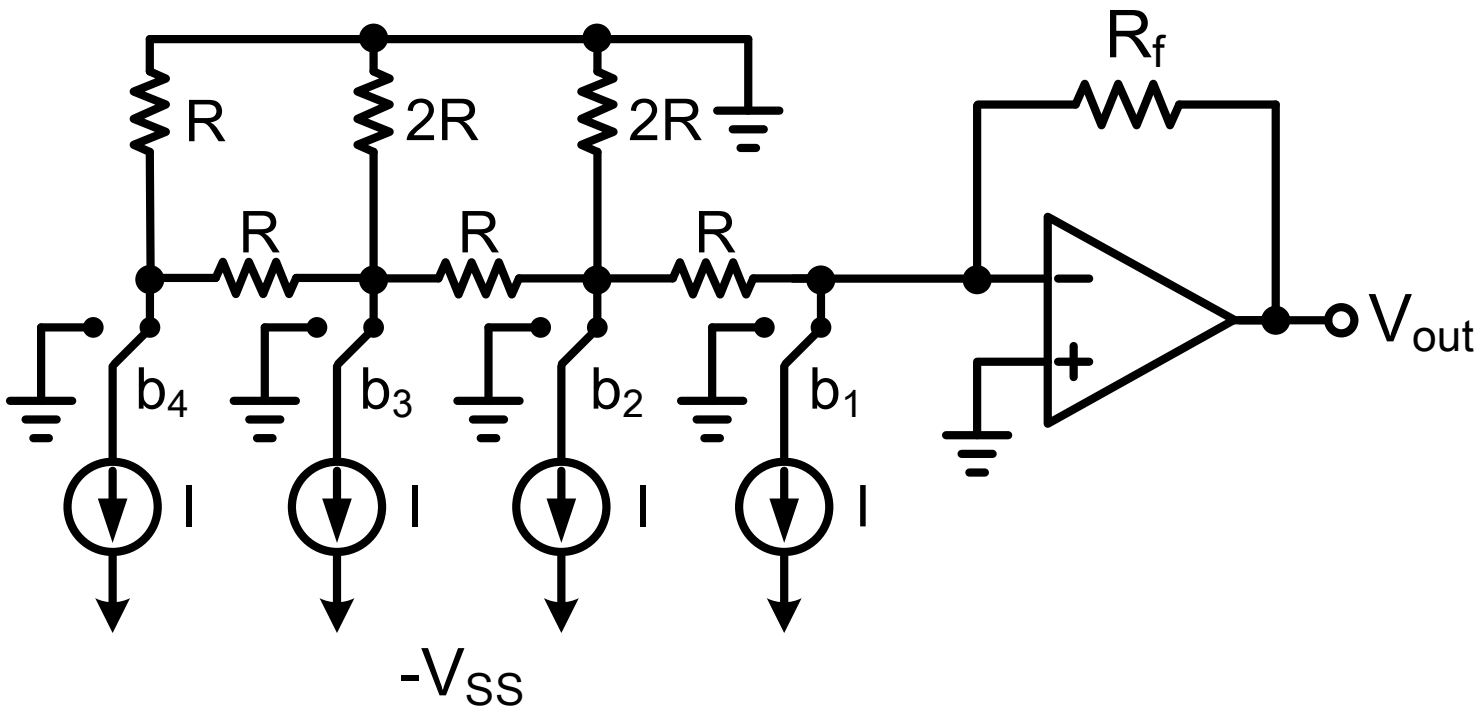
R-2R-Based DAC (Cont.)

- B_1 is 1 & all other bits are 0
  - $V_{out}=(R_F/R)(V_{ref}/2)$
- B_2 is 1 & all other bits are 0
  - $V_{out}=(R_F/R)(V_{ref}/4)$
- B_{N-1} is 1 & all other bits are 0
  - $V_{out}=(R_F/R)(V_{ref}/2^{N-1})$
- B_N is 1 & all other bits are 0
  - $V_{out}=(R_F/R)(V_{ref}/2^N)$

- Multiplying DAC (ref. p.12-47~12-48)
  - Use varying analog signal V_a instead of fixed reference voltage V_{ref}

R-2R-Based DAC (Cont.)

- R-2R ladder DAC with equal currents through switches
  - Slower since the internal nodes exhibit some voltage swings(as opposed to the previous configuration where internal nodes all remain at fixed voltage)



R-2R-Based DAC (Cont.)

- Assume only $b_1 = 1$, the current drawn through R_f is I

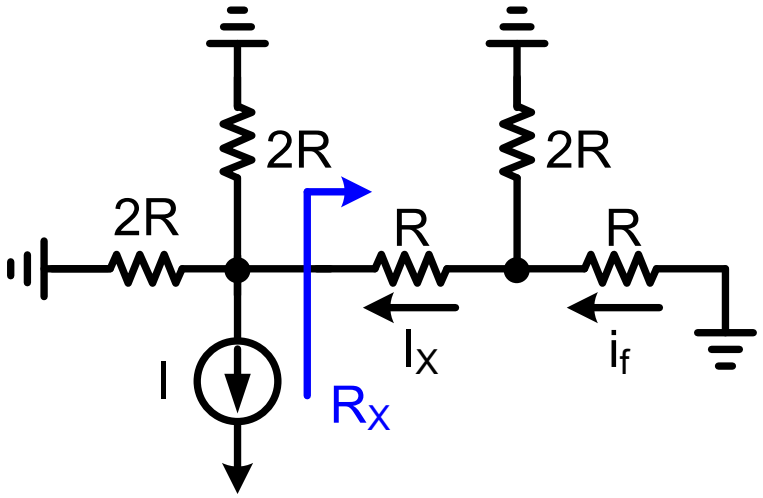
  Assume only $b_2 = 1$, the current drawn through R_f is $I/2$

  Assume only $b_3 = 1$, the equivalent circuitto find the current through R_f is:

$$R_X = R + \frac{2}{3}R = \frac{5}{3}R$$

$$I_X = I \times \frac{(2R||2R)}{(2R||2R)+\frac{5}{3}R} = \frac{3}{8}I$$

$$i_f = \frac{2R}{2R+R} I_X = \frac{1}{4}I$$

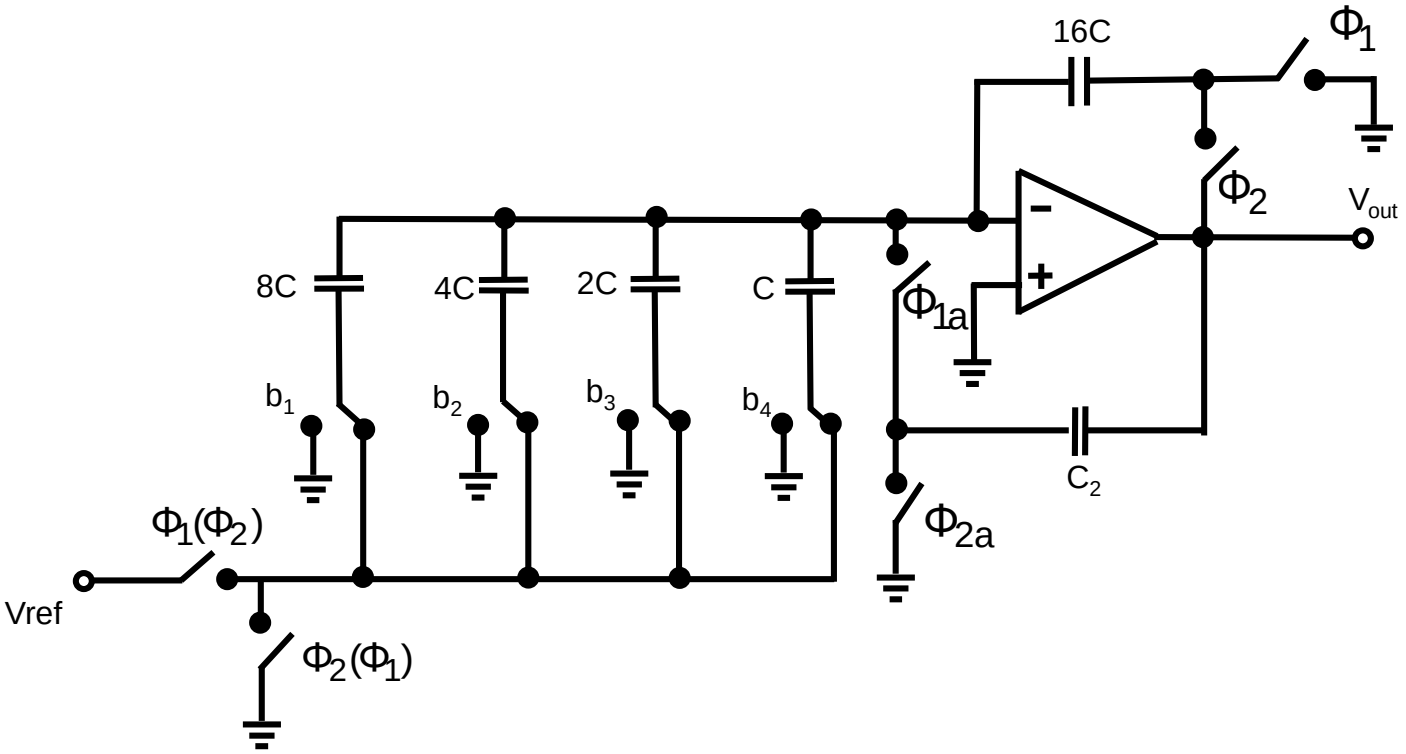


- With similar analysis, it can be shown that the current through b_4&R_f is $I/8$. Therefore,

$$V_{out} = 2R_f \times I(2^{-1}b_1 + 2^{-2}b_2 + 2^{-3}b_3 + 2^{-4}b_4)$$

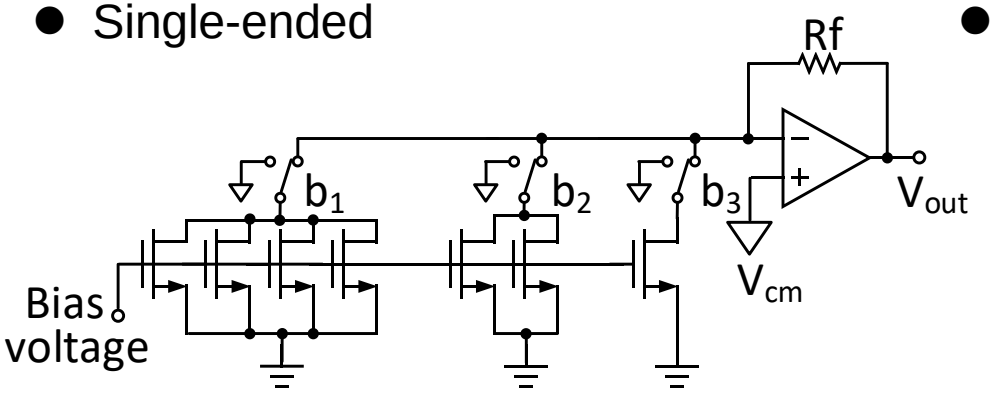
Charge-Redistribution Switched-Capacitor DAC

- Insensitive to OPAMP input-offset voltage, 1/f noise, and finite amplifier gain
- An additional sign bit can be realized by interchanging the clock phases (shown in parentheses)

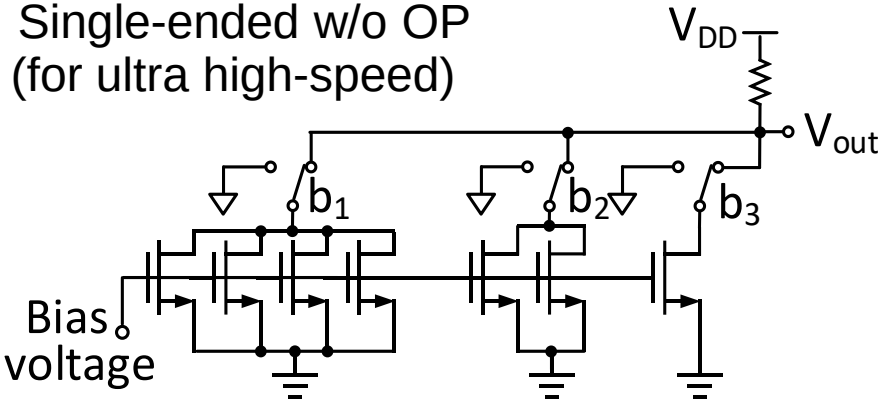


Current-Mode DAC

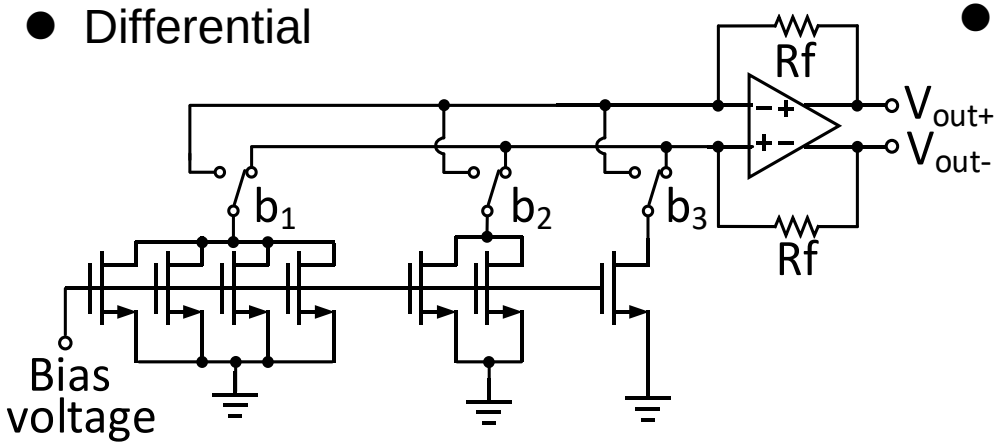
- High-speed
- Switch current to output or to ground
  The output current is converted to a voltage through R_F
- Upper portion of current source always remains at ground potential (w/ OP)
- Single-ended



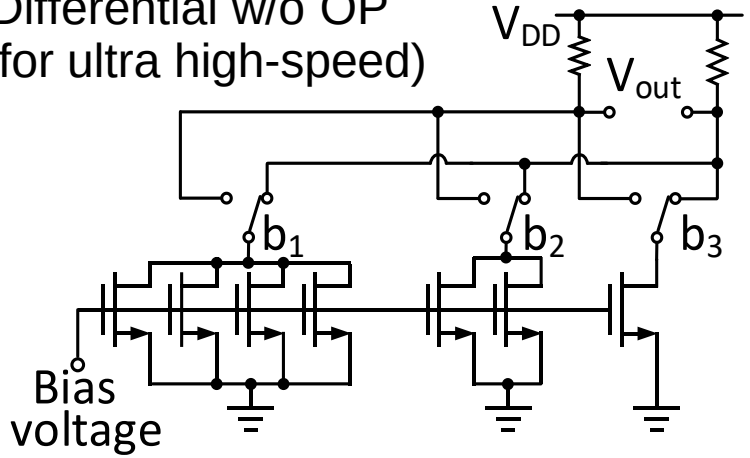
- Single-ended w/o OP
  (for ultra high-speed)



- Differential

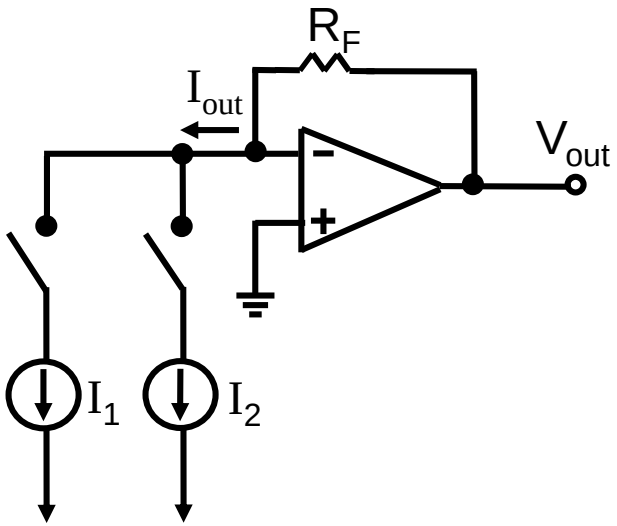


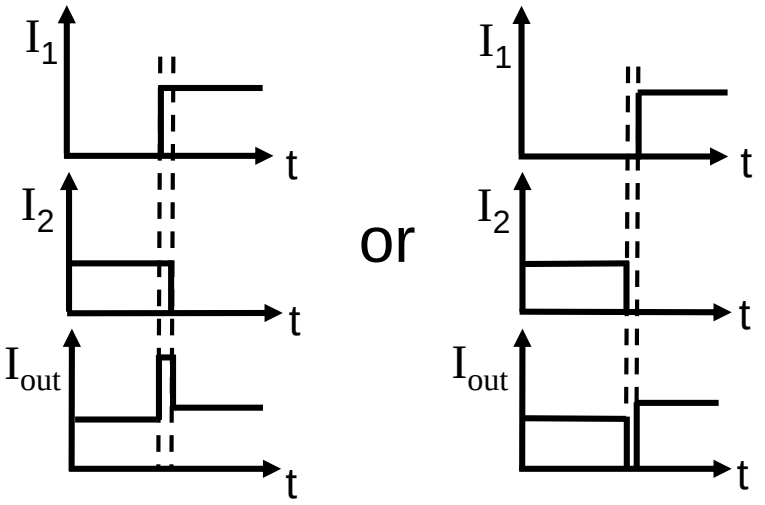
- Differential w/o OP
  (for ultra high-speed)



Glitches

- A major limitation during high-speed operation
- Mainly the result of different delays occuring when switching different signals
- Example: 01111……1--->1000 ……0
  - I_1 represents the MSB current, and I_2 represents the sum of (N-1) LSB currents.
  - MSB current turns off slightly early, causing a glitch of zero current





Glitches (Cont.)

- Glitch disturbance can be reduced by
  - Limiting the bandwidth (placing a capacitor across R_F)

    This method slows down the circuit.
  - Using a sample and hold on the output signal.
  - Modifying some or all of the digital word from a binary code to a thermometer code. (The most popular method.)

Thermometer-Code DACs

- Digitally recode the input to a thermometer-code equivalent

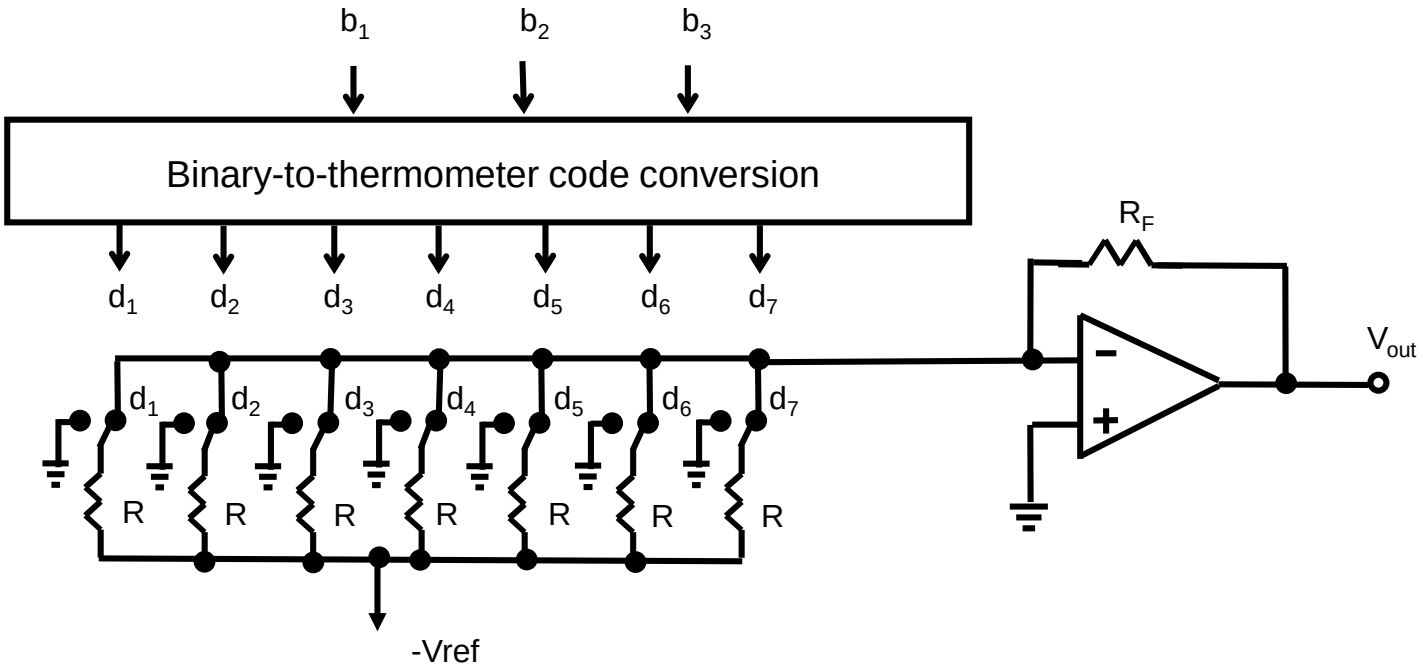
Thermometer-code representations for 3-bit binary values

Decimal	Binary			Thermometer Code						
	b1	b2	b3	d1	d2	d3	d4	d5	d6	d7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

- Advantages over its binary-weighted counterpart
  - Small DNL errors
  - Guaranteed monotonicity
  - Reduced glitching noise
- Does not increase the size of the analog circuitry compared to a binary-weighted approach

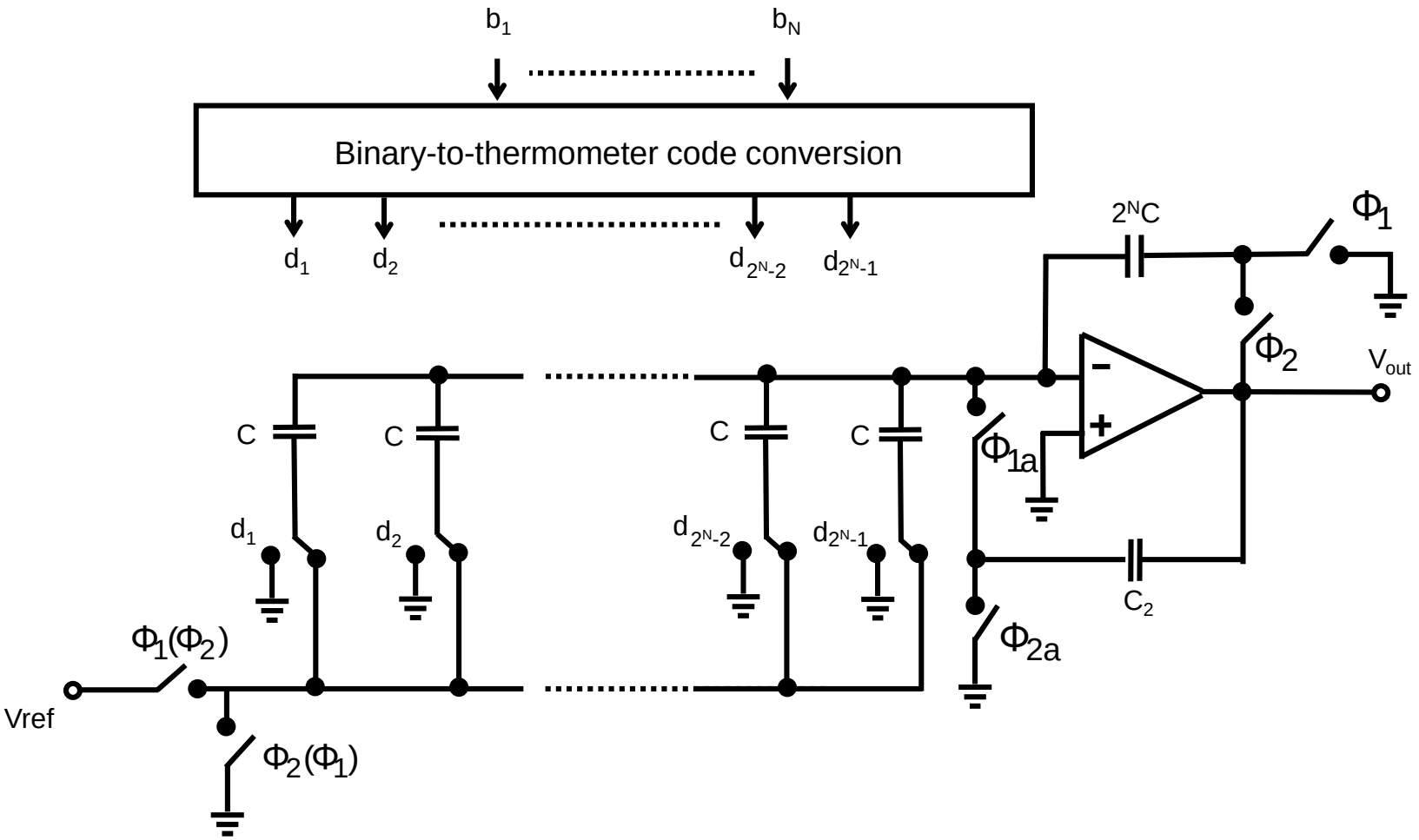
Thermometer-Code DACs (Cont.)

- Total area required by the transistor switches is the same (compared to binary-weighted)
  - All transistor switches are of equal sizes since they all pass equal currents
- Examples
  - Thermometer-code resistor DAC



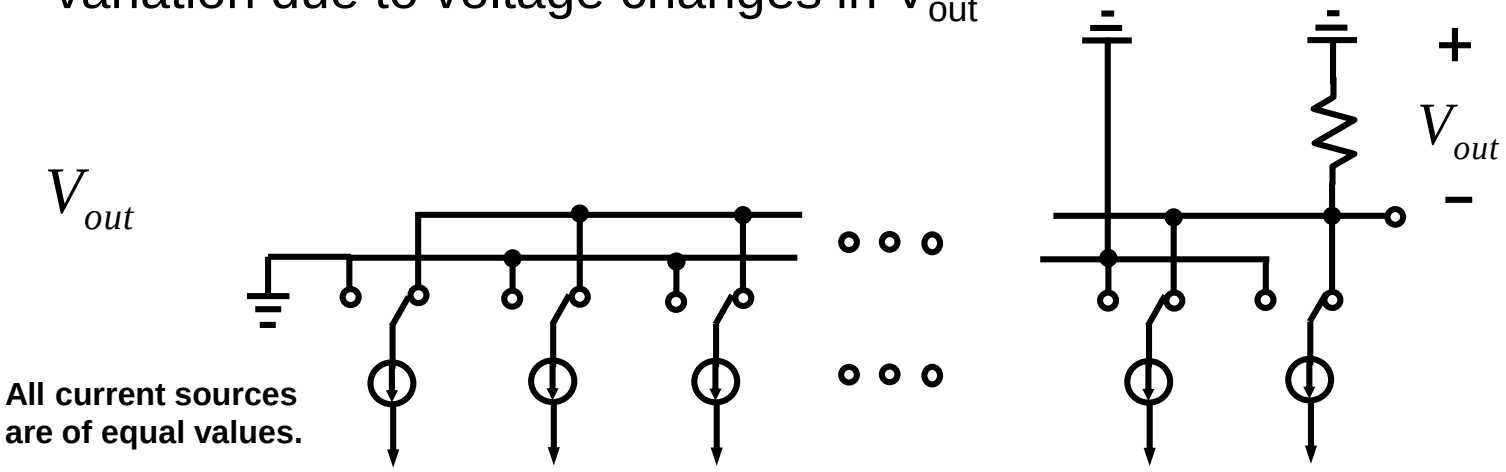
Thermometer-Code DACs (Cont.)

- Thermometer-code charge-redistribution DAC

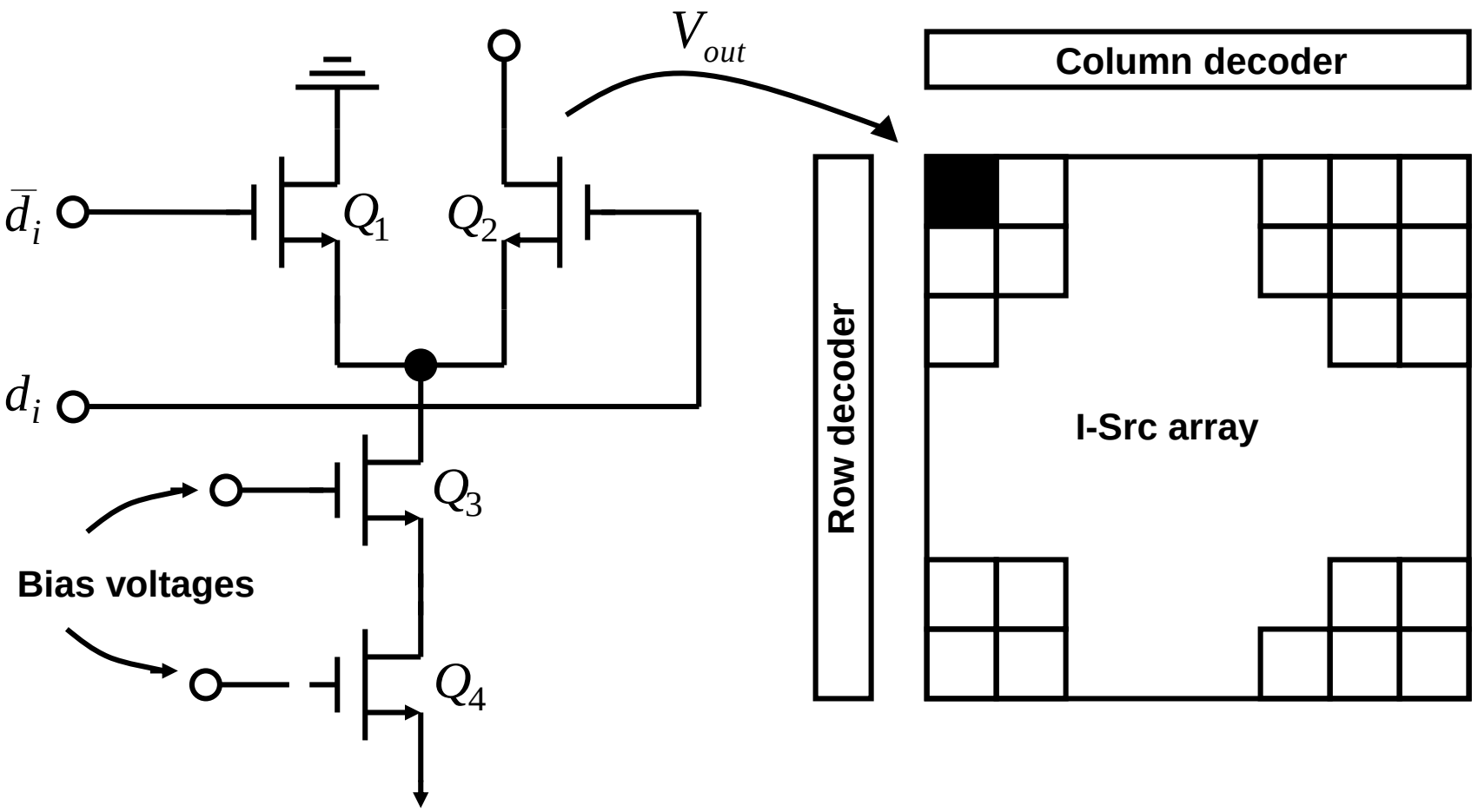


Thermometer-Code Current-Mode DAC

- Row and column decoders
- Inherent monotonicity
- Small DNL errors
  - INL errors depend on the placement of the current sources
- In high-speed applications
  - The output current feeds directly into an off-chip 50Ω or 75Ω resistor, rather than an output OPAMP.
  - Cascode current sources are used to reduce current-source variation due to voltage changes in V_{out}



Thermometer-Code Current-Mode DAC (Cont.)



[1] T. Miki, “An 80-MHz CMOS D/A converter,” IEEE J. Solid-State Circuits, vol. SC-21, no. 6, pp. 983-988, Dec. 1986.

[2] L. Letham, "Larsen, R.E.A high-performance CMOS 70-MHz palette/DAC", IEEE Journal of Solid-State Circuits, Volume 22, Issue 6, pp:1041-1047, Dec 1987.

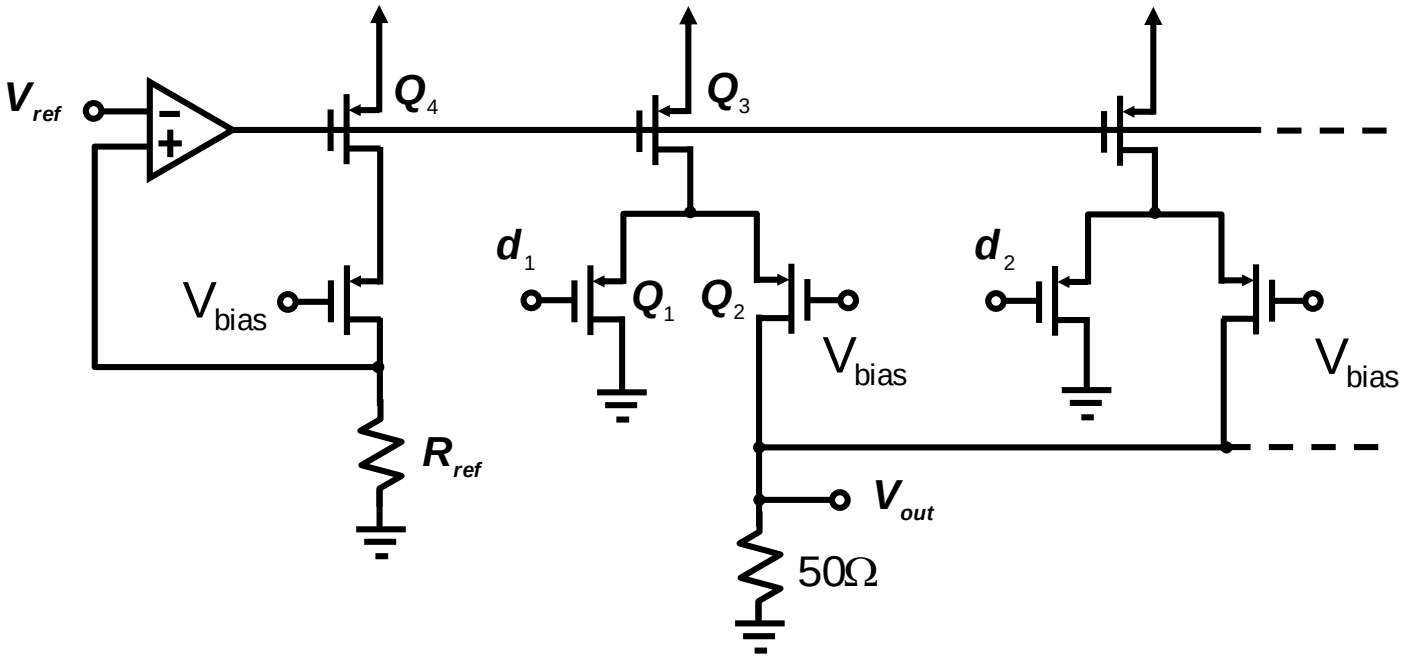
[3] K. K. Chi et al., “A CMOS triple 100Mbit/s video D/A converter with shift registers and color map,” IEEE J. Solid-State Circuits, vol. SC-21, no. 6, pp. 989-995, Dec. 1986

Thermometer-Code Current-Mode DAC (Cont.)

- Precisely timed edges are needed
  - If both $\overline{d}_i$ and d_i are low simultaneously, the drain of Q_3 is pulled low and the circuit takes longer time to respond.
  - If both $\overline{d}_i$ and d_i are high simultaneously, V_{out} is shorted to ground.

- To avoid the use of the two logic levels, the gate of Q_2 should be connected to a dc bias voltage

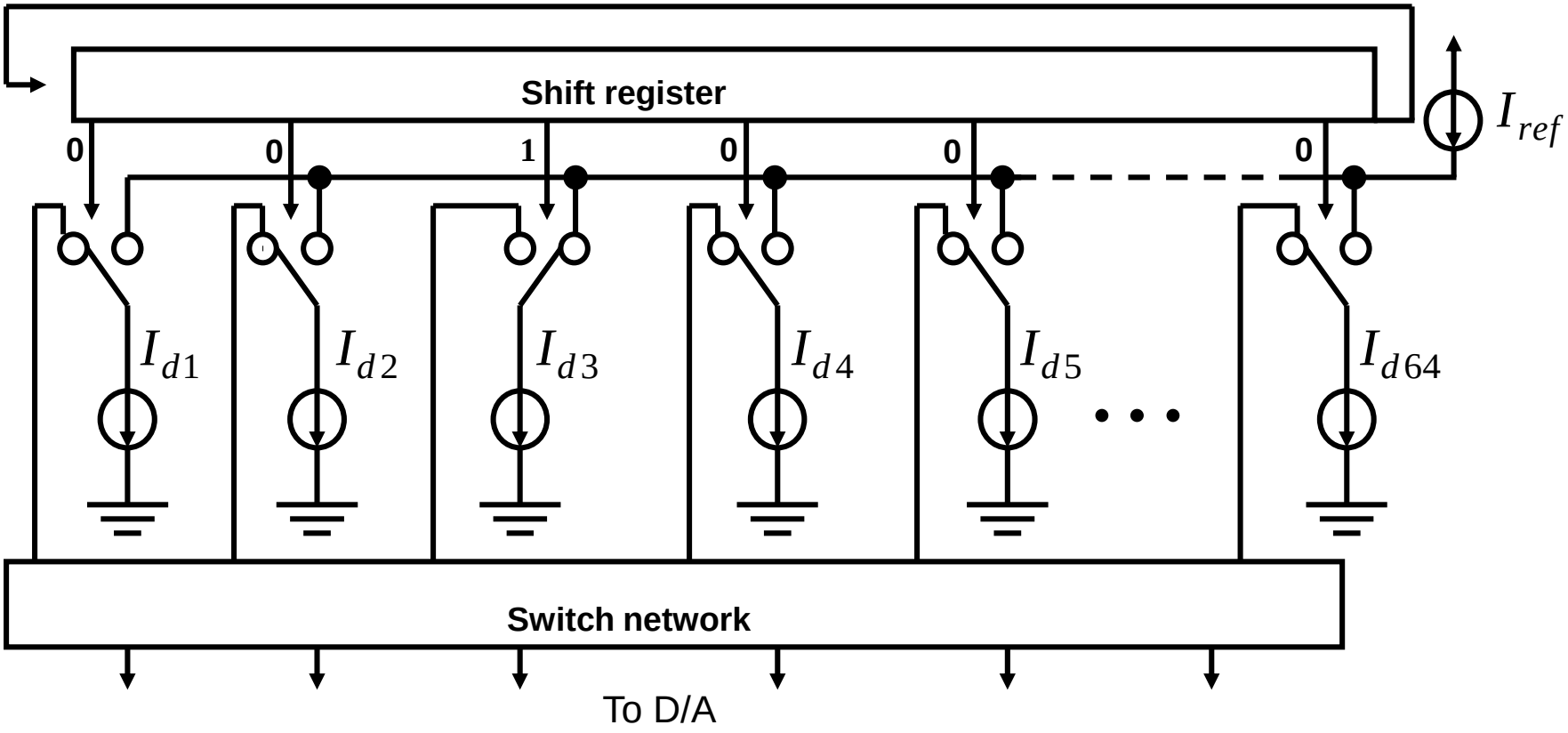
Thermometer-Code Current-Mode DAC (Cont.)



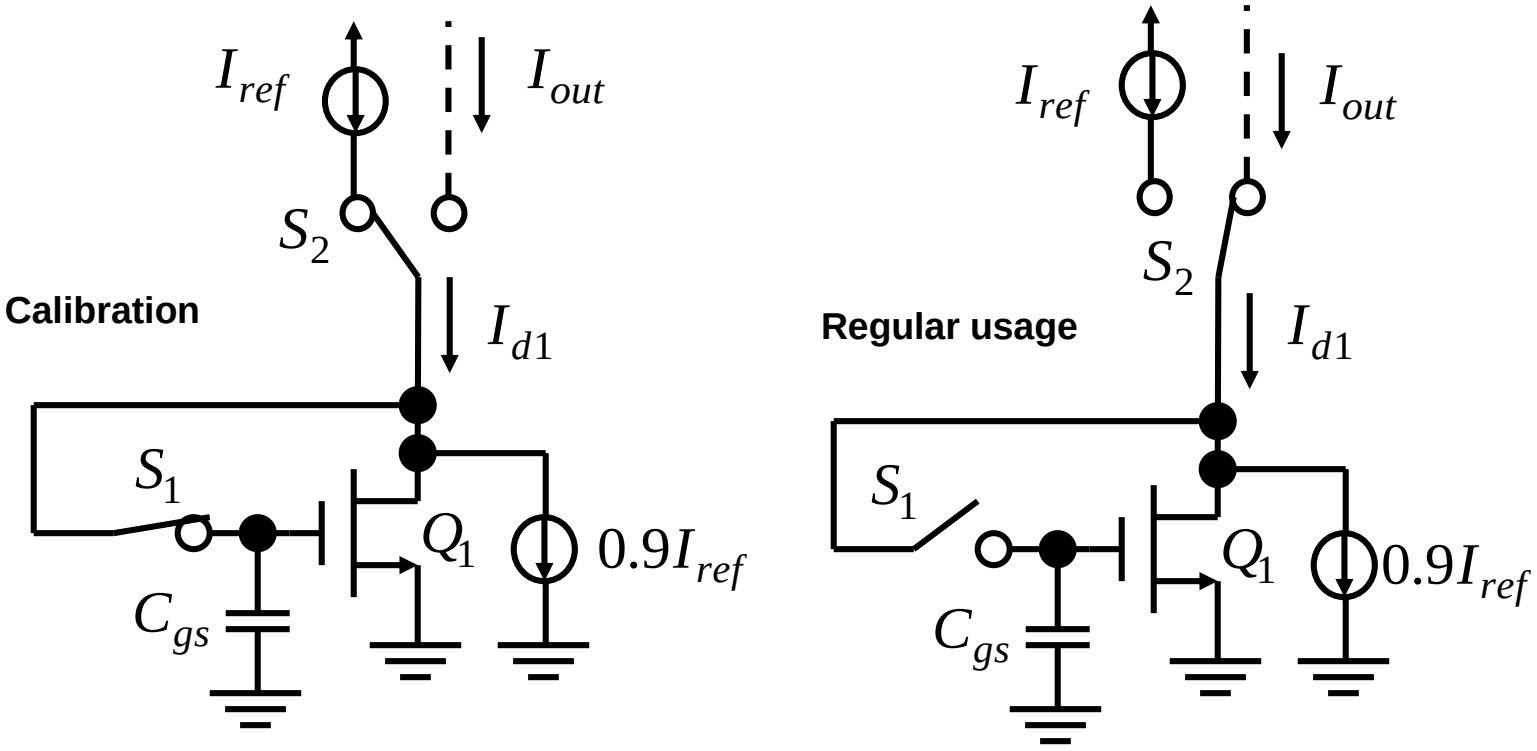
- Can be clocked at the maximum rate without the need for precisely timed edges
- Q_2 and Q_3 effectively form a cascode current source when they drive current to the output.
- To maximize speed, the voltage swing at the common connection (e.g. Q_1, Q_2 and Q_3) of the current switches should be small.

Dynamically Matched Current Sources

- A method for realizing very well-matched current sources (up to 16-bit accuracy) for audio DACs
- Continuously and cyclically calibrate MSB portions
- 16-bit example



Dynamically Matched Current Sources (Cont.)



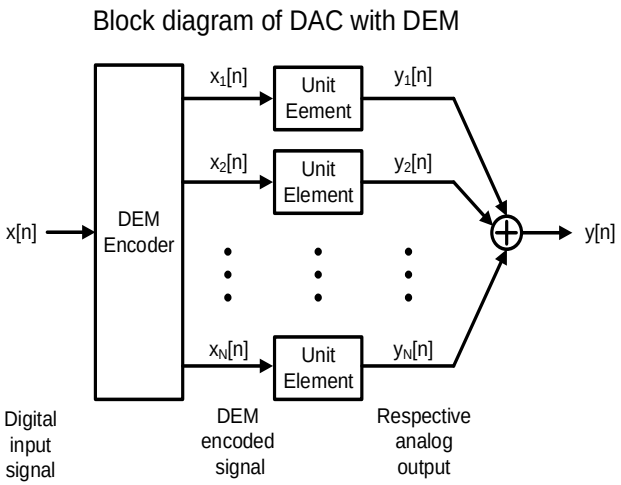
- 6MSBs were realized using a thermometer code
- Since the accuracy requirements are reduced for the remaining bits, a binary array was used in their implementation.

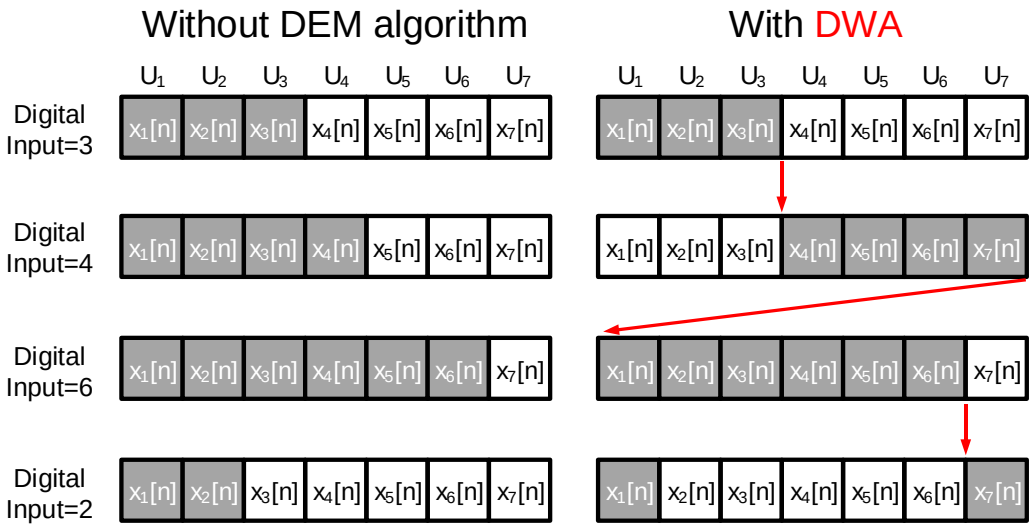
Dynamically Matched Current Sources (Cont.)

- 64 accurately matched current sources for the 6 MSBs
  - Current sources are calibrated
  - Dynamically setting current sources
  - Even though only 63 are required, the extra one is needed so that DAC can continuously operate when one of them is being calibrated
- Major limitation in matching 64 current sources is due to the differences in clock feedthrough and charge injection switches S_i
  - The best way is to minimize them
    - Large C_{gs} and large V_{gs} of Q_1
    - Q_1 only source a small current
    - W_{small} / L_{large} can be used for Q_1
- Large C_{gs} to minimize leakage current effect before current sources are recalibrated
- Dummy transistor can be added to S_i
- Other methods to minimize these errors are referred to switched-current (SI) papers

Dynamic Element Matching (DEM)

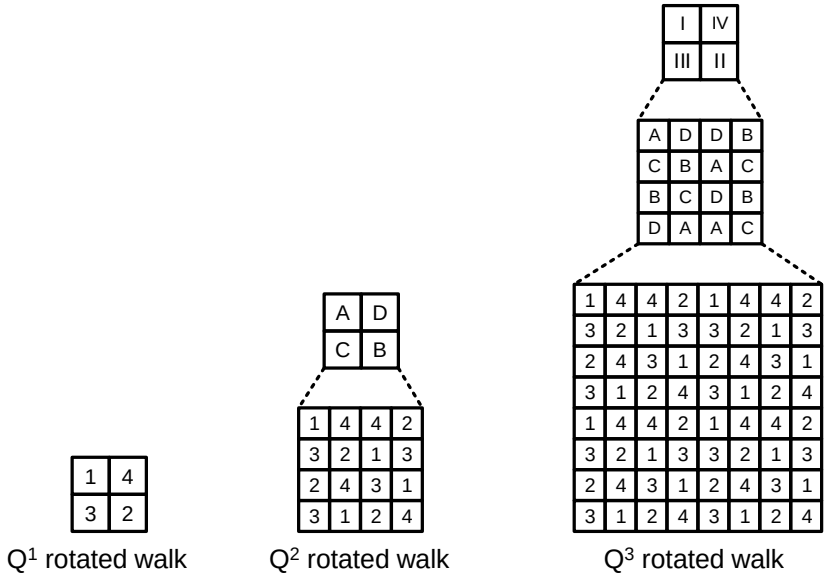
- Motivation: Repeated selection on the same mismatch elements
  → Accumulated error & Distortion
- DEM Policy: Balancing the selected times of each element
  - Reduction of repeated pattern → Eliminating distortion
  - Purely digital circuit for element selection → Scaling friendly
  - Less power and area consumption than calibration
- Popular DEM algorithms
  - Data weighted averaging (DWA)
  - DEM Randomization





Layout Placement for Gradient Error Compensation

- Gradient error → Mismatch between each current cell
- Layout technique to compensate gradient error
  - Partitioning of single current cell into multiple smaller segments
  - Balancing of current segments placement → Cancel mismatch
- Can be applied with DEM simultaneously for smaller output errors
- Example of a Q^N rotated walk switching scheme[1]



[1] D. Lee, Y. Lin, and T. Kuo, “Nyquist-rate current-steering digital-to-analog converters with random multiple data-weighted averaging technique and Q^N rotated walk switching scheme,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1264–1268, Nov. 2006.

Hybrid Converters

- Combine the advantages of different approaches
- It's quite common to use a thermometer-code approach for the top few MSBs while using a binary-scaled technique for the lower LSBs
  - Glitching is significantly reduced and accuracy is high
  - Circuit area is saved with a binary-scaled approach for LSBs
- Examples
  - Resistor-capacitor hybrid DAC (Refer to p.12-19)
  - Segmented DAC (Refer to textbook p.640)

1. The DAC is segmented into the 2 most significant bits (MSBs), 2 upper least significant bits (ULSBs) and 2 least significant bits (LSBs)
2. The current weighting of the segments are $I_{MSB}=16I_{LSB}$ and $I_{ULSB}=4I_{LSB}$